

IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of the claims in the application:

1. (Currently amended) A method for expanding the capacity of a fixed digital field for a model train control system, comprising:
  - providing a unique number field for a unique number calculated from the bits in said digital field;
  - calculating a first unique number from said digital field according to a first algorithm;
  - determining if said first unique number is present in said unique number field;
  - assigning a first meaning to a particular combination of bits in said digital field if said first unique number is present;
  - if said first unique number is not present, calculating a second unique number according to a second algorithm;
  - determining if said second unique number is present in said unique number field;
  - and
  - assigning a second meaning to said particular combination of bits in said digital field if said second unique number is present.
2. (Original) The method of Claim 1 further comprising:
  - indicating an error if neither said first nor said second unique number is present.
3. (Original) The method of Claim 1 wherein said particular combination of bits is a command.

4. (Original) The method of Claim 3 wherein said command is for an operation in a model train.

5. (Original) The method of Claim 4 wherein said command further includes an address of said model train.

6. (Original) The method of Claim 1 wherein said first unique number is a multiple bit code.

7. (Original) The method of Claim 6 wherein said second unique number is the inverse of said first unique number.

8. (Original) The method of Claim 1 wherein said unique number is an error code.

9. (Original) The method of Claim 1 wherein said fixed digital field is part of a transmission packet.

10. (Original) The method of Claim 1 wherein fill bits are used in transmission of said fixed digital field, and further comprising:

detecting said fill bits;

determining if said fill bits have a value other than a designated fill value;

if said fill bits have a value other than said designated fill value, assigning a different meaning to the combination of bits in said fixed digital field based on the value of said fill bits.

11. (Original) The method of Claim 10 further comprising:  
modifying a value of one of said fill bits, in accordance with the values of remaining ones of said fill bits, to minimize a DC offset of said transmission packet and fill bits.

12. (Original) The method of Claim 10 further comprising:  
utilizing at least one of said fill bits in calculating said second unique number.

13. (Original) The method of Claim 10 wherein said first unique number is a multiple bit code and said second unique number is the inverse of said first unique number.

14. (Original) A method for expanding the capacity of a fixed digital command field for a model train control system, comprising:

providing a multiple bit error code field for a unique number calculated from the command bits in said digital field;

calculating a first multiple bit error code from said digital field according to a first algorithm;

determining if said first multiple bit error code is present in said unique number field;

assigning a first meaning to a particular combination of bits in said digital field if said first multiple bit error code is present;

if said first multiple bit error code is not present, calculating a second multiple bit error code according to a second algorithm;

determining if said second multiple bit error code is present in said multiple bit error code field;

assigning a second meaning to said particular combination of bits in said digital field if said second multiple bit error code is present; and

indicating an error if neither said first nor said second multiple bit error code is present.

15. (Original) A method for expanding the capacity of a fixed digital command field for a model train control system, wherein the command field comprises four nibbles of four bits each, comprising:

- providing a multiple bit checksum field for a unique number calculated from the command bits in said digital field;

- calculating a first checksum from said command field by summing the values of each of said nibbles and dropping the most significant bit of the result;

- determining if said first checksum is present in said unique number field;
- assigning a first meaning to a particular combination of bits in said command field if said first checksum is present;

- if said first checksum is not present, calculating a second multiple bit error code according to a second algorithm;

- determining if said second multiple bit error code is present in said multiple bit error code field; and

- assigning a second meaning to said particular combination of bits in said command field if said second multiple bit error code is present; and

- indicating an error if neither said first nor said second multiple bit error code is present.

16. (Currently amended) An apparatus in a model train control system for receiving a digital field, comprising:

- a memory storing first and second algorithms;
- a processor, coupled to said memory;
- a program embodied in computer readable code in said memory, containing instructions configured to
  - detect a unique number field for a unique number calculated from the bits in said digital field;
  - calculate a first unique number from said digital field according to said first algorithm;
  - determine if said first unique number is present in said unique number field;
  - assign a first meaning to a particular combination of bits in said digital field if said first unique number is present;
  - if said first unique number is not present, calculate a second unique number according to a second algorithm;
  - determine if said second unique number is present in said unique number field;
  - and
  - assign a second meaning to said particular combination of bits in said digital field if said second unique number is present.

17. (Original) The apparatus of Claim 15 wherein said processor is a hardware FPGA.

18-22. (Cancelled)